

WEST[Help](#)[Logout](#)[Interrupt](#)[Main Menu](#)[Search Form](#)[Posting Counts](#)[Show S Numbers](#)[Edit S Numbers](#)[Preferences](#)[Cases](#)**Search Results -**

Terms	Documents
L5 and (HIGH or LOW) with logic	11

Database:
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09 1747, 734

Examiner: T. R. S. S. S.

Search:

L6 and user with defin\$4

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side by side

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result set

DB=USPT; PLUR=YES; OP=ADJ

<u>L6</u>	L5 and (HIGH or LOW) with logic	11	<u>L6</u>
<u>L5</u>	L4 and write with enable	12	<u>L5</u>
<u>L4</u>	L3 and fail\$3	13	<u>L4</u>
<u>L3</u>	L1 and control\$5 with input and process with corner	19	<u>L3</u>
<u>L2</u>	L1 and control\$5 with input and track\$3 with process with corners	0	<u>L2</u>
<u>L1</u>	integrated near circuit and test\$3 with (circuit or signal) and pulse with width	2873	<u>L1</u>

END OF SEARCH HISTORY

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Terms	Documents
test\$3 near SRAM and self with tim\$3 and write with stress	0

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Search:

L32

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DB=USPT; PLUR=YES; OP=ADJ

<u>L32</u>	test\$3 near SRAM and self with tim\$3 and write with stress	0	<u>L32</u>
<u>L31</u>	test\$3 near memory and self with tim\$3 and write with stress with mode	0	<u>L31</u>
<u>L30</u>	test\$3 with memory near device and self with tim\$3 with write with stress with mode	0	<u>L30</u>
<u>L29</u>	test\$3	719782	<u>L29</u>
<u>L28</u>	L26 and ((324/\$)!.CCLS.)	3	<u>L28</u>
<u>L27</u>	L26 and (built with in with test with circuit or BIST)	0	<u>L27</u>
<u>L26</u>	SRAM and test ADJ signal with pulse ADJ width	9	<u>L26</u>
<u>L25</u>	L23 and test ADJ signal with pulse ADJ width	0	<u>L25</u>

<u>L24</u>	L23 and ((324/\$)!.CCLS.)	0	<u>L24</u>
<u>L23</u>	L22 and HIGH near logic and LOW near logic	26	<u>L23</u>
<u>L22</u>	L21 and (SRAM or static with random with access with memory)	26	<u>L22</u>
<u>L21</u>	L15 and configuration with input	26	<u>L21</u>
<u>L20</u>	L15 and predict\$4 same fail\$4	0	<u>L20</u>
<u>L19</u>	L15 and predict\$4 with fail\$4	0	<u>L19</u>
<u>L18</u>	L15 and fuse	0	<u>L18</u>
<u>L17</u>	L15 and fuse same program\$5	0	<u>L17</u>
<u>L16</u>	L15 and fuse with program\$5	0	<u>L16</u>
<u>L15</u>	L14 and transition	26	<u>L15</u>
<u>L14</u>	L13 and user with program\$5	26	<u>L14</u>
<u>L13</u>	L12 and user with defin\$5	27	<u>L13</u>
<u>L12</u>	L11 and fail\$3	38	<u>L12</u>
<u>L11</u>	L10 and (HIGH or LOW) with logic	50	<u>L11</u>
<u>L10</u>	L8 and write with enable	55	<u>L10</u>
<u>L9</u>	L8 and process with corner\$4	0	<u>L9</u>
<u>L8</u>	L7 and control\$4 with input	88	<u>L8</u>
<u>L7</u>	L6 and pulse with width	102	<u>L7</u>
<u>L6</u>	BIST or (Built-in near test near circuit or built near in near test near circuit)	977	<u>L6</u>
<u>L5</u>	L4 and (HIGH or LOW) with logic	11	<u>L5</u>
<u>L4</u>	L3 and write with enable	12	<u>L4</u>
<u>L3</u>	L2 and fail\$3	13	<u>L3</u>
<u>L2</u>	L1 and control\$5 with input and process with corner	19	<u>L2</u>
<u>L1</u>	integrated near circuit and test\$3 with (circuit or signal) and pulse with width	2878	<u>L1</u>

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Terms	Documents
SRAM and test ADJ signal with pulse ADJ width	9

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Search:

L26 and (324/\$)!.CCLS.

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Set Name Query

side by side

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result set

DB=USPT; PLUR=YES; OP=ADJ

<u>L26</u>	SRAM and test ADJ signal with pulse ADJ width	9	<u>L26</u>
<u>L25</u>	L23 and test ADJ signal with pulse ADJ width	0	<u>L25</u>
<u>L24</u>	L23 and ((324/\$)!.CCLS.)	0	<u>L24</u>
<u>L23</u>	L22 and HIGH near logic and LOW near logic	26	<u>L23</u>
<u>L22</u>	L21 and (SRAM or static with random with access with memory)	26	<u>L22</u>
<u>L21</u>	L15 and configuration with input	26	<u>L21</u>
<u>L20</u>	L15 and predict\$4 same fail\$4	0	<u>L20</u>
<u>L19</u>	L15 and predict\$4 with fail\$4	0	<u>L19</u>
<u>L18</u>	L15 and fuse	0	<u>L18</u>
<u>L17</u>	L15 and fuse same program\$5	0	<u>L17</u>
<u>L16</u>	L15 and fuse with program\$5	0	<u>L16</u>
<u>L15</u>	L14 and transition	26	<u>L15</u>
<u>L14</u>	L13 and user with program\$5	26	<u>L14</u>
<u>L13</u>	L12 and user with defin\$5	27	<u>L13</u>
<u>L12</u>	L11 and fail\$3	38	<u>L12</u>
<u>L11</u>	L10 and (HIGH or LOW) with logic	50	<u>L11</u>
<u>L10</u>	L8 and write with enable	55	<u>L10</u>
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<u>L8</u>	L7 and control\$4 with input	88	<u>L8</u>
<u>L7</u>	L6 and pulse with width	102	<u>L7</u>
<u>L6</u>	BIST or (Built-in near test near circuit or built near in near test near circuit)	977	<u>L6</u>
<u>L5</u>	L4 and (HIGH or LOW) with logic	11	<u>L5</u>
<u>L4</u>	L3 and write with enable	12	<u>L4</u>
<u>L3</u>	L2 and fail\$3	13	<u>L3</u>
<u>L2</u>	L1 and control\$5 with input and process with corner	19	<u>L2</u>
<u>L1</u>	integrated near circuit and test\$3 with (circuit or signal) and pulse with width	2878	<u>L1</u>

END OF SEARCH HISTORY